Bd of appeal

Docket No.: SON-2047
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Akihiko Koh et al.

Appeal No. 2009-004407

Application No.: 09/802,857

Confirmation No.: 3304

Filed: March 12, 2001

Art Unit: 2192

For: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM

Examiner: M. J. Yigdall

AMENDMENT AFTER DECISION ON APPEAL UNDER 37 CFR 41.50

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Decision on Appeal dated May 14, 2010:

The option pursuant to 37 C.F.R. §41.50 for the **reopening of prosecution** is exercised.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

AMENDMENTS TO THE CLAIMS

1-26. (Canceled)

27. (Currently amended) A data processing apparatus comprising:

a bug address setting register adapted to store a bug address, said bug address indicating ~~an~~ a start address for a buggy part of a program; ~~data;~~

a coincidence detecting circuit adapted to compare ~~said~~ a program address with said bug address and output an interrupt request signal, said interrupt request signal indicating ~~coincidence or non~~ a coincidence ~~of~~ between said program address and said bug address;

a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal; and

a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates ~~a~~ said coincidence. ~~between said address and said bug address.~~

28. (Previously presented) A data processing apparatus as set forth in claim 27, wherein said value is incremented when said interrupt request signal indicates said coincidence.

29-39. (Canceled)

40. (Currently amended) A data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a bug address setting register adapted to store a bug address, said bug address indicating a starting address within said program memory for a buggy part of said program; and

a counter register adapted to store a value, said value being incremented when ~~representing a number of times~~ an interrupt request signal indicates a coincidence between said program address and said bug address,

wherein another program address indicates a location within said program memory for another of the instruction codes. ~~, and~~

~~wherein said value of the counter register is incremented by 1.~~

41-44. (Canceled)

45. (Currently amended) A data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal;

a first coincidence detecting circuit adapted to compare said program address with a first bug address and output said first interrupt request signal, said central processing unit receiving said first interrupt request signal;

a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal, said central processing unit receiving said second interrupt request signal;

a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,

wherein said counter register is set to 0 during ~~said~~ initialization processing.

46. (Previously presented) A data processing apparatus as set forth in claim 45, wherein said counter register is located within a random access memory at a predetermined memory address.

47. (Previously presented) A data processing apparatus as set forth in claim 45, further comprising:

bug address setting registers adapted to store said first and second bug addresses.

48. (Previously presented) A data processing apparatus as set forth in claim 45, wherein said first bug address indicates a starting address within said program memory for a first buggy part

of said program, and said second bug address indicates a starting address within said program memory for a second buggy part of said program.

49. (Previously presented) A data processing apparatus as set forth in claim 48, wherein said central processing unit is adapted use said value to select for correction said first buggy part or said second buggy part.

50. (Previously presented) A data processing apparatus as set forth in claim 45, wherein said first and second interrupt request signals are input to said central processing unit as two different interrupt request signals.

51. (Previously presented) A data processing apparatus as set forth in claim 45, wherein said first and second interrupt request signals are input to said central processing unit as a single interruption.

52. (Previously presented) A data processing apparatus as set forth in claim 51, wherein said first and second interrupt request signals are AND'ed together to become said single interruption.

REMARKS

This is in full and timely response to the Decision on Appeal dated May 14, 2010.

Claims 27-28, 40 and 45-52 are currently pending in this application, with claims 27, 40 and 45 being independent.

No new matter has been added.

Reexamination in light of the following remarks is respectfully requested.

Option to reopen prosecution is exercised

i. The option pursuant to 37 C.F.R. §41.50 for the reopening of prosecution is exercised.

Pursuant to 37 C.F.R. §41.50(b), when the Board makes a new ground of rejection, the appellant, within two months from the date of the decision, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

(1) Reopen prosecution.

(2) Request rehearing.

The new ground of rejection is binding upon the examiner unless an amendment or new evidence not previously of record is made which, in the opinion of the examiner, overcomes the new ground of rejection stated in the decision. 37 C.F.R. §41.50(b).

This Amendment is believed to overcome the new ground of rejection stated in the Decision. 37 C.F.R. §41.50(b)(1).

Rejections within the Final Office Action of December 28, 2007

i. Rejections within the Final Office Action of December 28, 2007.

A. Paragraph 6 of the Office Action indicates a rejection of claims 45-52 under 35 U.S.C. §112, second paragraph.

B. Paragraph 8 of the Office Action indicates a rejection of claims 27-28 and 40 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,784,537 to Suzuki et al. (Suzuki).

C. Paragraph 9 of the Office Action indicates a rejection of claims 45-50 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal) and in view U.S. Patent No. 5,784,537 (Suzuki).

D. Paragraph 10 of the Office Action indicates a rejection of claims 51 and 52 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal), and in view U.S. Patent No. 5,784,537 (Suzuki), and in further view U.S. Patent No. 5,701,506 (Hosotani).

Reversal of the rejection of claims 27-28, 40 and 45-52

i. The Decision indicates a *reversal* of the rejections within the Final Office Action of December 28, 2007.

Page 4 of the Decision provides that:

> *For the reasons set forth subsequently in this opinion, with respect to all claims on appeal, claims 27, 28, 40, and 45 through 52, the existing prior art rejections must be reversed pro forma because they are necessarily based on speculative*

assumptions and inferences as to the meaning of the claims. See In re Steele, 305 F.2d 859,862-863 (CCPA 1962).

New ground of rejection under 35 U.S.C. §112, second paragraph

i. Claims 27-28 and 40.

While not conceding the propriety of the new ground of rejection and in order to advance the prosecution of the present application, claims 27-28 and 40 have been amended in accordance with the Decision.

ii. Claim 45.

A. Standard of review.

An applicant for patent is entitled to select the claim language as long as the meaning is reasonably plain and specific. *Ellipse Corporation v. Ford Motor Company*, 312 F.Supp. 646, 660, 164 USPQ 161, 171 (N.D. Ill. 1969).

The plain meaning of claims language is entitled to a strong presumption that it correctly expresses the scope of the claim. *In re Certain Thermometer Sheath Packages* , 205 USPQ 932, 941 (ITC 1979).

When a patentee explicitly defines a claim term in the patent specification, the patentee's definition controls. *Martek Biosciences Corp. v. Nutrinova Inc.*, 92 USPQ2d 1148, 1159 (Fed. Cir. 2009).

A patentee can be his own lexicographer provided the patentee's definition, to the extent it differs from the conventional definition, is clearly set forth in the specification. *Beachcombers v. Wildewood Creative Prods., Inc.*, 31 USPQ2d 1653, 1656 (Fed. Cir. 1994).

For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *General Electric Co. v. Nintendo Co.*, 50 USPQ2d 1910, 1914 (Fed. Cir. 1999).

The following description is provided for illustrative purposes and is not intended to limit the scope of the invention.

B. Page 5 of the Decision asserts the following:

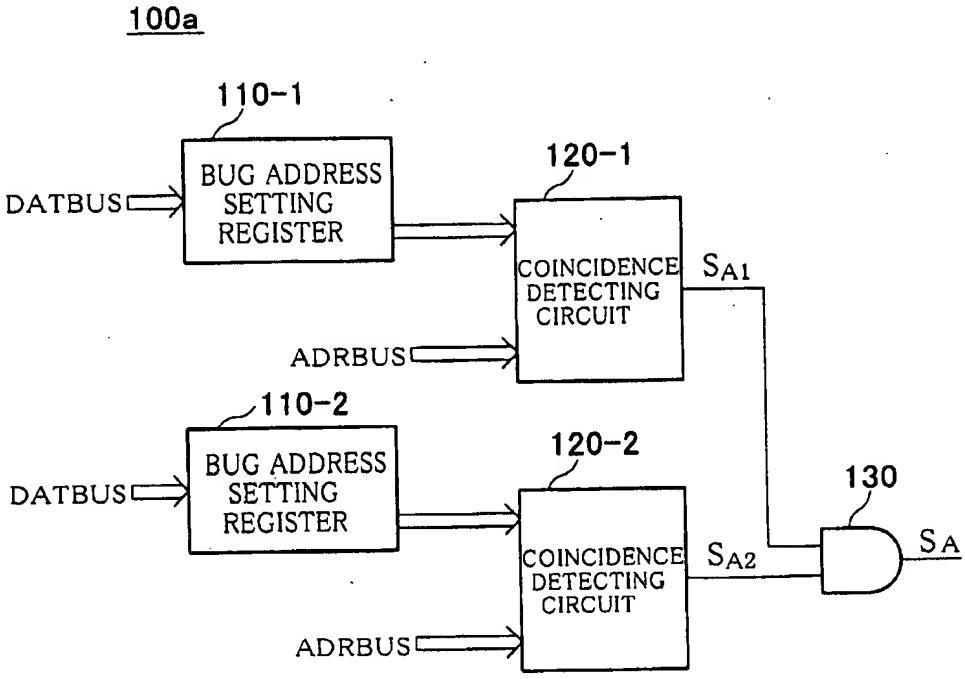
> ***Lastly, we turn to independent claim 45. This claim has several recitations of first and second as applied to interrupt request signals, coincidence detecting circuits, bug addresses, and the like among several interrelated clauses.***
>
> ***The claim fails to specify that the first and second recitations in the various clauses are with respect to different entities or elements.***
>
> ***The first and second recitations may apply to a single given circuit element at different points in time.***
>
> ***These ambiguities alone appear to cause the claim to be read in different degrees of scope and in different manners.***

In response, Figure 7 of the specification for the instant application is block diagram of a second embodiment of the data processing apparatus according to the present invention and showing the configuration of the debugging circuit.

Claim 45 is drawn to a data processing apparatus comprising:	Paragraphs within U.S. Patent Application Publication No. 2001/0052114, the publication document for the present application.
program memory (30) adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;	Paragraphs [0050], [0051]
a central processing unit (10) adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of **a first interrupt request signal (S_{A1})** or **a second interrupt request signal (S_{A2})**;	Paragraph [0054]
a first coincidence detecting circuit (120-1) adapted to compare said program address with **a first bug address** and output *said first interrupt request signal (S_{A1})*, said central processing unit (10) receiving *said first interrupt request signal (S_{A1})*;	Paragraph [0066], [0073]
a second coincidence detecting circuit (120-2) adapted to compare said program address with **a second bug address** and output *said second interrupt request signal (S_{A2})*, said central processing unit (10) receiving *said second interrupt request signal (S_{A2})*;	Paragraph [0066], [0073]
a counter register adapted to store a value, said value being incremented by 1 when *said first interrupt request signal* indicates a coincidence between said address and *said first bug address* or when said *second interrupt request signal* indicates a coincidence between said address and *said second bug address*,	Paragraph [0075]
wherein said counter register is set to 0 during initialization processing.	Paragraph [0075]

For convenience, Figure 7 of the specification as originally filed is shown hereinbelow.

FIG.7



C. Page 5 of the Decision asserts the following:

> ***The claim also does not recite, as the Examiner aptly indicates in the Examiner's own rejection under § 112 second paragraph, the actual recitation of an initialization processing to which the last clause, the wherein clause, refers when it states "said initialization processing."***

While not conceding the propriety of the new ground of rejection and in order to advance the prosecution of the present application, claim 45 has been amended in accordance with the Decision.

Conclusion

This response is believed to be a complete response to the Decision on Appeal.

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

Dated: June 4, 2010

Respectfully submitted,

By_____

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AMENDMENT TRANSMITTAL LETTER

Docket No. SON-2047

Application No.	Filing Date	Examiner	Art Unit
09/802,857-Conf. #3304	March 12, 2001	M. J. Yigdall	2192

Applicant(s): Akihiko Koh et al.

Invention: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	11	- 20 =	0	x 52.00	0.00
Independent Claims	3	- 3 =	0	x 220.00	0.00
Multiple Dependent Claims (check if applicable)	☐				
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00

☒ Large Entity ☐ Small Entity

☒ No additional fee is required for this amendment.

☐ Please charge Deposit Account No. _____ in the amount of $ _____.

☐ A check in the amount of $ _____ to cover the filing fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge and credit Deposit Account No. 18-0013 as described below. A duplicate copy of this sheet is enclosed.

☒ Credit any overpayment.

☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Dated: June 4, 2010

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